REMARKS

The claims have been amended to more clearly define the invention as disclosed in the written description. In particular, claims 17, 24 and 25 have been amended for clarity.

Applicant believes that the above changes answer the Examiner's 35 U.S.C. 112, paragraph 2, rejection of claims 24 and 25, and respectfully requests withdrawal thereof.

The Examiner has rejected claims 17 and 18 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 6,052,295 to Buchschacher et al. The Examiner has further rejected claims 19 and 26-28 under 35 U.S.C. 103(a) as being unpatentable over Buchschacher et al. in view of U.S. Patent 6,986,151 to Lenssen et al. In addition, the Examiner has rejected claims 20-23 under 35 U.S.C. 103(a) as being unpatentable over Buchschacher et al. in view of Lenssen et al., and further in view of U.S. Patent 5,567,976 to Dierschke et al. Furthermore, the Examiner has rejected claims 24 and 25 under 35 U.S.C. 103(a) as being unpatentable over Buchschacher et al. in view of Lenssen et al. and Dierschke et al., and further in view of U.S. Patent 5,955,687 to Miyagi et al.

The Buchschacher et al. patent discloses a cascade of voltage multipliers, which, as noted by the Examiner, includes "an electronic circuit comprising conversion means (see Fig. 1 and col 1 lines65-67) for converting an input voltage (U_i, col 2 line 4) into an output voltage (U_o, col 2 line 14), comprising at least a first energy storage means (a first capacitor C1, col 2 line 55)

and a second energy storage means (output capacitor C_{out}, col 4 line 6) and switching means (Sw1, Sw2, Sw3, Sw4 and Sw5, Fig. 2) for periodically coupling said energy storage means (C1, C2) to one another under the control of a clock signal so as to store energy in the energy storage means (C1, C2) and transferring at least a portion of the stored energies between the energy storage means".

As noted in MPEP §2131, it is well-founded that "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California,* 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Further, "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.,* 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

The subject invention, as claimed in claim 1, includes the limitation "clock signal generating means for generating the clock signals, said control signal generating means simultaneously keeping all of the clock signals in holding states during a holding period during operation, said holding states being equal to the states of the respective clock signals immediately before the holding period".

The Examiner has indicated that this is taught by Buchschacher et al., and states "(The first charge pump CHGPMP1 further comprises a first capacitor C1 and a first buffer BF1 having an input for receiving the clock input signal d1, col 2

lines 54-60)."

Applicant submits that while what the Examiner is attributing to Buchschacher et al. is correct, this is not what is claimed in claim 17. In particular, claim 17 claims "switching means for periodically coupling, under control of clock signals, said at least first and second energy storage means to one another so as to store energy in the at least first and second energy storage means, and for transferring at least a portion of the stored energies between the at least first and second energy storage means" As such, the clock signals control the switching means. The clock input signal d1 of Buchschacher et al. does not control the switching means, but rather is used by the charge pump to control the application of a charge to the capacitor C1.

As described in the subject specification on page 8, lines 7-13, if the input voltage is intermittent for holding periods RT, the control signals need to be generated differently. In the case of Buchschacher et al., the control signals would be changed to de-activate all of the voltage multipliers. Instead, in the subject invention, as claimed, all of the clock signals are simultaneously placed into holding states during the holding period, wherein the holding states are "equal to the states of the respective clock signals immediately before the holding period".

The Lenssen et al. patent discloses an information carrier, apparatus, substrate, and system, in which an information carrier is provided with a storage unit, an integrated circuit and a coupling element. However, Applicant submits that Lenssen et al.

does not provide that which is missing from Buchschacher et al., i.e., "clock signal generating means for generating the clock signals, said clock signal generating means simultaneously keeping all of the clock signals in holding states during a holding period during operation, said holding states being equal to the states of the respective clock signals immediately before the holding period".

The Dierschke et al. patent discloses a position sensing photosensor device, in which an integrated circuit includes an array of photosensitive sensors for detecting a position of an incident light spot.

With regard to claim 20, the Examiner then states "the use of photosensitive sensors in ICs is well known in the art, and as an example Dierschke teaches integrated circuits including photosensitive sensors. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the electronic circuit of Buchschacher to have a photosensitive sensor thereby to control the input voltage based on the quantity of light."

Applicant submits, however, that as specifically claimed in claim 20, the photosensitive sensor of the subject invention is being used to generate (or provide) the input voltage, not to control the input voltage.

Further, Dierschke et al. does not supply that which is missing from Buchschacher et al. and Lenssen et al., i.e., "clock signal generating means for generating the clock signals, said

clock signal generating means simultaneously keeping all of the clock signals in holding states during a holding period during operation, said holding states being equal to the states of the respective clock signals immediately before the holding period".

The Miyagi et al. patent discloses a disc music box, information disc therefor, and trick timepiece with disc music box, which discloses the use of a light sensor which outputs a voltage or a current signal corresponding to the variable quantity of received light.

The Examiner then states "It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the medium taught by Buchschacher, Lenssen and Dierschke to be able to control the holding period using a photosensitive sensor that regulated voltage based on the amount of light received."

Applicant submits that the combination of Buchschacher et al., Lenssen et al. and Dierschke et al. does not disclose or suggest a holding period during which all of the clock signals are simultaneously put in holding states. The benefit of this is described in the specification on page 2, lines 2-18. With regard to Miyagi et al., Applicant submits that it is common knowledge that the output voltage from a light sensor varies with the amount of light. However, this combined with Buchschacher et al., Lenssen et al. and Dierschke et al. has no bearing on what is done by the clock generating means during a holding period.

Further, Applicant submits that Miyagi et al. does not supply that which is missing from Buchschacher et al. in view of Lenssen et al. and Dierschke et al., i.e., "clock signal generating means for generating the clock signals, said clock signal generating means simultaneously keeping all of the clock signals in holding states during a holding period during operation, said holding states being equal to the states of the respective clock signals immediately before the holding period".

In view of the above, Applicant believes that the subject invention, as claimed, is neither anticipated nor rendered obvious by the prior art, either individually or collectively, and as such, is patentable thereover.

Applicant believes that this application, containing claims 17-28, is now in condition for allowance and such action is respectfully requested.

Respectfully submitted,

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